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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
HENRY, MATTHEW ALLAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,244	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-40 are rejected under the judicially created doctrine of double patenting over corresponding claims 1-40 of U. S. Patent No. 6,715,018 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: Both the patent and pending application are directed to communicating between cards in a computer system through a direct fiber-optic communication link.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Specification

3. The disclosure is objected to because of the following informalities:

Examiner feels the statement made in Paragraph 24 is superfluous as it is inherent to an application for a U.S. Patent that the proposed invention is meant to "promote the process of science and useful arts."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 8, 24-28 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwa (4,863,232).

Regarding Claim 1, Kwa discloses:

A system comprising:

a housing (Figure 1, Item 110);

a circuit board supported in the housing (Figure 1, Item 114);

a plurality of slot connectors supported on the circuit board (Figure 1, Item 116);

a first card in one of the slot connectors (Figure 1, Item 140);

a first circuit component mounted on the first card (Column 1, Lines 11-22);

a second card in another one of the slot connectors (Figure 1, Item 140);

a second circuit component mounted on the second card (Column 1, Lines 11-22); and

an optical interconnect coupling the first card to the second card (Figure 1, Item 130), the first circuit component being configured to communicate with the second circuit component via the optical interconnect (Column 1, Lines 11-22), whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

Regarding Claim 8, Kwa discloses:

A system comprising:

a housing (Figure 1, Item 110);

a circuit board supported in the housing (Figure 1, Item 114);

a slot connector supported on the circuit board (Figure 1, Item 116);

a first circuit component supported by the circuit board (Figure 1, Item 140; Column 1, Lines 11-22; the circuit board supports a card which supports the first circuit component);

a card removably received (Column 4, Lines 29-30) in one of the slot connectors (Figure 1, Item 140);

a second circuit component mounted on the card (Column 1, Lines 11-22); and

an optical interconnect coupling the card to the circuit board (Figure 1, Item 130), the first circuit component being configured to communicate with the second circuit component via the optical interconnect (Column 1, Lines 11-22), whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

Regarding Claims 2, 25 and 40, Kwa further discloses:

optically coupling the first card to the second card comprises using a fiber optic cable (Figure 1, Item 130).

Regarding Claims 3-5 and 26-28, Kwa further discloses:

the optical interconnect comprises a first optical connector, on the first card, configured to convert between electrical signals and optical signals, wherein the computer further includes circuit traces on the first card coupling the first optical connector to the first circuit component, wherein the optical interconnect further comprises an optical connector, on the second card, configured to convert between electrical signals and optical signals, the computer further including circuit traces on the second card coupling the second optical connector to the second circuit component (Column 1, Lines 11-22; the first and second cards have transmitting and receiving circuitry connected to further circuitry crafted in this matter).

Regarding Claim 24, Kwa discloses:

A method of assembling a system, the method comprising:

supporting a circuit board (Figure 1, Item 114) in a housing (Figure 1, Item 110);

supporting a plurality of slot connectors on the circuit board (Figure 1, Item 116);

mounting a first circuit component (Column 1, Lines 11-22) on a first card (Figure 1, Item 140);

inserting the first card into a first one of the slot connectors (Column 4, Lines 29-30);

mounting a second circuit component (Column 1, Lines 11-22) on a second card (Figure 1, Item 140);

inserting the second card into a second one of the slot connectors (Column 4, Lines 29-30); and

flexibly optically coupling the first card to the second card for optical communications between the first circuit component and the second circuit component (Figure 1, Item 130; Column 1, Lines 11-22; the optical coupling is clearly flexible in the figure), whereby the flexible optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

Regarding Claim 39, Kwa discloses:

A system comprising:

a housing (Figure 1, Item 110);

a circuit board supported in the housing (Figure 1, Item 114);

a plurality of slot connectors supported on the circuit board (Figure 1, Item 116);

a first card (Figure 1, Item 140) configured for sliding receipt (Column 4, Lines 29-30) in one of the slot connectors;

a first circuit component mounted on the first card (Column 1, Lines 11-22);

a second card (Figure 1, Item 140) configured for sliding receipt (Column 4, Lines 29-30)in one of the slot connectors;

a second circuit component mounted on the second card (Column 1, Lines 11-22); and

an optical interconnect coupling the first card to the second card (Figure 1, Item 130), the first circuit component being configured to communicate with the second circuit component via the optical interconnect (Column 1, Lines 11-22), whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 7, 11-16, 18-21, 23, 29-33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa (4,863,232) in view of Kimmel (4,704,599) and Gillingham (*SLDRAM: High-Performance Open-Standard Memory).*

Regarding Claims 6, 7, 12, 13, 29 and 30, Kimmel teaches:

the first or second circuit component comprises a memory (Column 2, Lines 19-22).

Kimmel is motivated to allow for the removal of a single card in a system containing a plurality of such cards without affecting the remainder of the system (Column 1, Lines 34-38).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the teaching of Kimmel into the system disclosed by Kwa for the benefit of allowing single cards in the multiple card system to be removed without affecting the performance of the remainder of the system.

Kimmel does not specify the memory device to be a DRAM or a SLDRAM memory device.

Gillingham teaches:

Synchronous link DRAM (Pages 29-39).

Gillingham states, "SLDRAM meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards" (Page 29, Column 1, Paragraph 2).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to further combine the teachings of SLDRAM as presented by Gillingham into the system so as to make use of memory that can support emerging processor architecture while still maintaining a low degree of cost.

Regarding Claim 11, Kwa further discloses:

the optical interconnect comprises an optical connector on the card configured to convert between electrical signals and optical signals, and an optical connector on the circuit board configured to convert between electrical signals and optical signals (Column 1, Lines 11-22).

Regarding Claims 14, 19, 31 and 35, Kwa discloses:

A method and a computer comprising:

supporting a circuit board (Figure 1, Item 114) in a housing (Figure 1, Item 110);

supporting a plurality of slot connectors (Figure 1, Item 116) on the circuit board (Figure 1, Item 114);

supporting a first circuit component (Column 1, Lines 11-22) on a first card (Figure 1, Item 140) having an edge connector (Figure 1, Item 142);

inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board (Column 4, Lines 29-30);

providing a second card (Figure 1, Item 140) having an edge connector (Figure 1, Item 142) configured for sliding receipt in a second one of the slot connectors (Column 4, Lines 29-30);

supporting a second circuit component (Column 1, Lines 11-22) on a second card having an edge connector;

inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board (Column 4, Lines 29-30);

Kwa does not specify the circuit components to be a processor and a SLDRAM memory. Further, Kwa does not provide details as to how the circuitry is powered.

optically coupling the first circuit component to the second circuit component for data communications using an optical interconnect within the housing (Figure 1, Item 130; Column 1, Lines 11-22), wherein the optical interconnect does not pass through the slot connectors (Column 1, Lines 51-62).

Kimmel teaches:

Having insertable cards with supporting a processor and a memory (Column 2, Lines 19-22).

supporting a power supply in the housing (Column 1, Lines 17-19);

coupling the power supply to the processor via the first slot connector (Figure 3, Item 106), the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the processor (Figure 3, Item 64);

coupling the power supply to the memory via the second slot connector (Figure 3, Item 106), the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the memory (Figure 3, Item 64); and

Kimmel is motivated to allow for the removal of a single card in a system containing a plurality of such cards without affecting the remainder of the system (Column 1, Lines 34-38).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the teaching of Kimmel into the system disclosed by Kwa for the benefit of allowing single cards in the multiple card system to be removed without affecting the performance of the remainder of the system.

Kimmel does not specify the memory device to be a SLDRAM memory device.

Gillingham teaches:

Synchronous link DRAM (Pages 29-39).

Gillingham states, "SLDRAM meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards" (Page 29, Column 1, Paragraph 2).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to further combine the teachings of SLDRAM as presented by Gillingham into the system so as to make use of memory that can support emerging processor architecture while still maintaining a low degree of cost.

Regarding Claims 15, 20, 32 and 36, Kimmel further teaches:

a third card in a third one of the connectors (Figure 1, Item 18), a co-processor supported by the third card (Column 2, Lines 19-22).

Kimmel does not teach coupling the co-processor and processor with an optical interconnect.

Kwa further discloses:

an optical interconnect coupling a first circuit component to the second circuit component (Figure 1, Item 130; Column 1, Lines 11-22).

Regarding Claims 16, 21, 33 and 37, Kimmel further teaches:

conductors coupling the power supply to the co-processor via the third connector (Figure 3, Item 106) , the conductors including circuit traces on the third card (Figure 3, Item 64).

Regarding Claims 18 and 23, Kwa further discloses:

including an electronic device in the housing capable of generating electromagnetic interference (Figure 1, Item 142), and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference (Figure 1, Item 142; the electric connections are capable of generating interference, which, by virtue of the optical connection being disposed apart from these electrical connections, are substantially inhibited from interfering with the memory/process intercommunications).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa (4,863,232) in view of Fish (5,845,107).

Regarding Claim 9, Fisch teaches:

the first circuit component (Figure 2, Item 206) is hard wired to the circuit board (Figure 2, Item 201; Column 4, Lines 44-46).

Fisch is motivated to allow for the interfacing of a variety of different busses over a high speed bus (Column 4, Lines 46-49).

Accordingly, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Fisch wherein a component mounted on a motherboard may be connected to communicate with a component mounted on a daughtercard with the system presented by Kwa for the benefit of allowing different processors to communicate over a high speed optical bus.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa (4,863,232) in view of Goldberg (4,352,536).

Regarding Claim 10, Goldberg teaches:

a ZIF connector mounted to the circuit board, and wherein the first circuit component (Figure 5a, Item 12) is removably received in the ZIF connector (Figure 1, Item 1).

Goldberg is motivated to use ZIF connectors because they minimize the amount of force needed to connect a circuit board to a system (Column 1, Lines 14-17).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate ZIF connectors as taught by Goldberg with the system disclosed by Kwa for the benefit of allowing circuit boards to be inserted with minimal force.

10. Claims 17, 22, 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa (4,863,232), Kimmel (4,704,599) and Gillingham (*SLDRAM: High-Performance Open-Standard Memory)* in further view of Freedman (4,839,829).

Regarding Claims 17, 22, 34 and 38, Freedman teaches:

a math co-processor (Column 5, Lines 66-68).

Freedman uses a math coprocessor to enhance floating point computational speeds (Column 5, Lines 66-68).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate a math co-processor as taught by Freedman into the system taught by Kwa, Kimmel and Gillingham for the benefit of enhance floating point computational speeds.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Block (4,850,044) discloses optically coupling adjacent cards and circumventing communication through the electrical connectors of the cards.

Corfield (4,682,323) discloses optically communicating with circuits.

Hirabayashi (JP 09005581) appears to depict direct optical connection of circuit boards.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday-Tuesday, Thursday-Friday (8:00 am -6:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100